CLAIMS

What is claimed is:

1. A method for semiconductor device feature development using a bi-layer photoresist comprising the steps of:

providing a non-silicon containing photoresist layer over a substrate;

providing a silicon containing photoresist layer over the non-silicon containing photoresist layer;

exposing an exposure surface of the silicon containing photoresist layer to an activating light source said exposure surface defined by an overlying pattern according to a photolithographic process;

developing the silicon containing photoresist layer according to a photolithographic process to reveal a portion the non-silicon containing photoresist layer; and

dry developing said non-silicon containing photoresist layer in a plasma reactor by igniting a plasma from an ambient mixture including at least nitrogen and oxygen.

2. The method of claim 1, wherein the plasma reactor includes at least one RF power source for plasma excitation and at least one RF power source for accelerating plasma generated ions towards the substrate surface.

3. The method of claim 1, wherein the non-silicon containing photoresist layer comprises a non-photoactive polymer.

4. The method of claim 1, wherein the ambient mixture includes about 1 part oxygen and about 1 to about 100 parts nitrogen, a remaining balance of said ambient mixture further including Argon to total 3~100 parts.

5. The method of claim 1, wherein the activating light source has a wavelength of one of about 157 nanometers and about 193 nanometers.

6. The method of claim 1, wherein the non-silicon containing photoresist layer has a thickness greater than the silicon containing photoresist layer.

7. The method of claim 6, wherein the non-silicon containing photoresist layer has a thickness of about 1000 Angstroms to about 5000 Angstroms and the silicon containing photoresist layer has a thickness of about 500 Angstroms to about 3000 Angstroms.

8. The method of claim 2, further comprising the step of removing the silicon containing photoresist layer according to a first in-situ ashing process following the step including dry developing.

9. The method of claim 8, wherein the first in-situ ashing process includes igniting an oxygen containing plasma said oxygen containing plasma further including at least one of nitrogen and fluorine ions said oxygen containing plasma being optimized to simultaneously clean plasma contact surfaces.

10. The method of claim 8, further comprising the step of etching a semiconductor feature through at least a portion of the substrate according to a reactive ion etch process.

11. The method of claim 10, wherein the semiconductor feature includes at least one of a via hole, a trench line, a contact hole, a shallow trench isolation feature, and a polysilicon gate feature.

12. The method of claim 10, further comprising the step of removing the non-silicon containing photoresist layer according to a second in-situ ashing process.

13. The method of claim 12, wherein the second in-situ ashing process further includes igniting an oxygen containing plasma further including at least one of nitrogen and fluorine, the oxygen containing plasma being optimized to simultaneously clean plasma contact surfaces.

14. The method of claim 13, wherein the second in-situ cleaning process includes maintaining the oxygen containing plasma at an ambient pressure of about 5 to about 1000 mTorr, supplying power to the first RF power source at about 200 to about 5000 Watts, and supplying power to the second RF power source at about 50 to about 500 Watts.

15. The method of claim 13, further comprising the step of reactively ion etching through a thickness of a metal nitride layer included in the substrate using a hydrofluorocarbon containing plasma to at least partially form the semiconductor feature.

16. The method of claim 15, further comprising the step of performing an in-situ cleaning process including igniting an oxygen containing plasma further including at least one of nitrogen and fluorine said oxygen containing plasma being optimized to clean plasma contact surfaces.

17. The method of claim 16, wherein the in-situ cleaning process includes operating the oxygen containing plasma at an ambient pressure of about 5 to about 1000 mTorr, supplying power to the first RF power source at about 200 to about 5000 Watts, and supplying power to the second RF power source at about 50 to about 500 Watts.

18. The method of claim 12, wherein the step including the first in-situ ashing process is combined with the step including the second in-situ ashing process following the step of etching the semiconductor feature to remove the silicon containing photoresist layer and the non-silicon containing photoresist layer.

19. The method of claim 10, wherein the step of the step of etching a semiconductor feature further includes etching through an insulating layer with a dielectric constant of less than about 3 included in the substrate.

20. The method of claim 12, wherein the steps including dry developing, the first in-situ ashing process, the reactive ion etch process, the second in-situ-ashing process, and the in-situ cleaning process are carried out in the plasma reactor according to a continuous process.